IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claim 1 (Currently Amended): A random number's seed generating circuit comprising:

an oscillator which generates a clock; and

a counter which operates in synchronism with the clock, wherein a count value of said counter is output in response to a signal asynchronous with the clock, and the [output] count value is used as an initial value to generate a random number, and

wherein said oscillator comprises a voltage-controlled oscillator having an external terminal, said oscillator and said external terminal are electrically disconnected before the count value is output, and said oscillator and said external terminal are electrically connected after the count value is output.

Claim 2 (Original): A circuit according to claim 1, wherein the signal is a signal output from a power-on reset circuit upon detecting that a power supply is turned on, and a power supply potential is stabilized.

Claim 3 (Original): A circuit according to claim 1, wherein the signal is an operation start signal output from a controller.

Claim 4 (Original): A circuit according to claim 3, wherein the operation start signal is output when the controller recognizes that a power supply is turned on.

Claim 5 (Original): A circuit according to claim 3, wherein the operation start signal is output when the controller recognizes that a predetermined operation is performed by a user.

Claim 6 (Original): A circuit according to claim 1, wherein said oscillator is set in an inoperative state or lowers a frequency of the clock after the count value is output in response to the signal.

Claim 7 (Canceled).

Claim 8 (Original): A circuit according to claim 7, wherein a switch circuit controlled by the signal is connected between said oscillator and the external terminal.

Claim 9 (Original): A circuit according to claim 7, wherein after the count value is output, the clock is used as a system clock.

Claim10 (Original): A circuit according to claim 1, wherein a timing at which the count value is output changes within a range of time longer than a period of the clock every time the count value is output.

Claim 11 (Original): A circuit according to claim 1, further comprising a latch circuit which latches the count value on the basis of the signal, wherein the count value latched by said latch circuit is used as the initial value.

Claim 12 (Original): A circuit according to claim 1, wherein when a random number generating circuit to which the signal is input is set in an operative state, the count value is simultaneously received by the random number generating circuit as the initial value.

Claim 13 (Currently Amended): A random number's seed generating circuit comprising:

an oscillator which generates a clock; and

a counter which operates in synchronism with the clock,

wherein a timing at which a count value of said counter is output changes at random within a predetermined range in response to a signal, and the [output] count value is used as an initial value to generate a random number, and

wherein said oscillator comprises a voltage-controlled oscillator having an external terminal, said oscillator and said external terminal are electrically disconnected before the count value is output, and said oscillator and said external terminal are electrically connected after the count value is output.

Claim 14 (Original): A circuit according to claim 13, wherein the signal is a signal output from a power-on reset circuit upon detecting that a power supply is turned on, and a power supply potential is stabilized.

Claim 15 (Original): A circuit according to claim 13, wherein the signal is an operation start signal output from a controller.

Claim 16 (Original): A circuit according to claim 15, wherein the operation start signal is output when the controller recognizes that a power supply is turned on.

Claim 17 (Original): A circuit according to claim 15, wherein the operation start signal is output when the controller recognizes that a predetermined operation is performed by a user.

Claim 18 (Original): A circuit according to claim 13, wherein said oscillator is set in an inoperative state or lowers a frequency of the clock after the count value is output in response to the signal.

Claim 19 (Canceled).

Claim 20 (Original): A circuit according to claim 19, wherein a switch circuit controlled by the signal is connected between said oscillator and the external terminal.

Claim 21 (Original): A circuit according to claim 19, wherein after the count value is output, the clock is used as a system clock.

Claim 22 (Original): A circuit according to claim 13, wherein a timing at which the count value is output changes within a range of time longer than a period of the clock every time the count value is output.

Claim 23 (Original): A circuit according to claim 13, further comprising a latch circuit which latches the count value on the basis of the signal, wherein the count value latched by said latch circuit is used as the initial value.

Claim 24 (Original): A circuit according to claim 13, wherein when a random number generating circuit to which the signal is input is set in an operative state, the count value is simultaneously received by the random number generating circuit as the initial value.

Claim 25 (Currently Amended): A driver comprising:

a random number's seed generating circuit having an oscillator which generates a clock and a counter which operates in synchronism with the clock; and

a random number generating circuit which generates a random number using an initial value generated by said random number's seed generating circuit,

wherein a count value of said counter is output in response to a signal asynchronous with the clock, the [output] count value is used as the initial value, and transfer data is kept secret using the random number, and

wherein said oscillator comprises a voltage-controlled oscillator having an external terminal, said oscillator and said external terminal are electrically disconnected before the count value is output, and said oscillator and said external terminal are electrically connected after the count value is output.

Claim 26 (Original): A driver according to claim 25, wherein the random number is generated every time a power supply is turned on, every time the data is written or read, or every time a predetermined operation is performed by
a user.

Claim 27 (Original): A driver according to claim 25, wherein the signal is a signal output from a power-on reset circuit upon detecting that a power supply is turned on, and a power supply potential is stabilized.

Claim 28 (Original): A driver according to claim 25, wherein the signal is an operation start signal output from a controller.

Claim 29 (Original): A driver according to claim 28, wherein the operation start signal is output when the controller recognizes that a power supply is turned on.

Claim 30 (Original): A driver according to claim 28, wherein the operation start signal is output when the controller recognizes that a predetermined operation is performed by a user.

Claim 31 (Original): A driver according to claim 25, wherein said oscillator is set in an inoperative state or lowers a frequency of the clock after the count value is output in response to the signal.

Claim 32 (Canceled).

Claim 33 (Original): A driver according to claim 32, wherein a switch circuit controlled by the signal is connected between said oscillator and the external terminal.

Claim 34 (Original): A driver according to claim 32, wherein after the count value is output, the clock is used as a system clock.

Claim 35 (Original): A driver according to claim 25, wherein a timing at which the count value is output changes within a range of time longer than a period of the clock every time the count value is output.

Claim 36 (Original): A driver according to claim 25, further comprising a latch circuit which latches the count value on the basis of the signal,

wherein the count value latched by said latch circuit is used as the initial value.

Claim 37 (Original): A driver according to claim 25, wherein when said random number generating circuit to which the signal is input is set in an operative state, the count value is simultaneously received by said random number generating circuit as the initial value.

Claim 38 (Currently Amended): A driver comprising:

a random number's seed generating circuit having an oscillator which generates a clock and a counter which operates in synchronism with the clock and

a random number generating circuit which generates a random number using an initial value generated by said random number's seed generating circuit,

wherein a timing at which a count value of said counter is output changes at random within a predetermined range in response to a signal, the [output] count value is used as the initial value, and transfer data is kept secret using the random number, and

wherein said oscillator comprises a voltage-controlled oscillator having an external terminal, said oscillator and said external terminal are electrically disconnected before the count value is output, and said oscillator and said external terminal are electrically connected after the count value is output.

Claim 39 (Original): A driver according to claim 38, wherein the random number is generated every time a power supply is turned on, every time the data is written or read, or every time a predetermined operation is performed by a user.

Claim 40 (Original): A driver according to claim 38, wherein the signal is a signal output from a power-on reset circuit upon detecting that a power supply is turned on, and a power supply potential is stabilized.

Claim 41 (Original): A driver according to claim 38, wherein the signal is an operation start signal output from a controller.

Claim 42 (Original): A driver according to claim 41, wherein the operation start signal is output when the controller recognizes that a power supply is turned on

Claim 43 (Original): A driver according to claim 41, wherein the operation start signal is output when the controller recognizes that a predetermined operation is performed by a user.

Claim 44 (Original): A driver according to claim 38, wherein said oscillator is set in an inoperative state or lowers a frequency of the clock after the count value is output in response to the signal.

Claim 45 (Canceled).

Claim 46 (Original): A driver according to claim 45, wherein a switch circuit controlled by the signal is connected between said oscillator and the external terminal.

Claim 47 (Original): A driver according to claim 45, wherein after the count value is output, the clock is used as a system clock.

Claim 48 (Original): A driver according to claim 38, wherein a timing at which the count value is output changes within a range of time longer than a period of the clock every time the count value is output.

Claim 49 (Original): A driver according to claim 38, further comprising a latch circuit which latches the count value on the basis of the signal, wherein the count value latched by said latch circuit is used as the initial value.

Claim 50 (Original): A driver according to claim 38, wherein when said random number generating circuit to which the signal is input is set in an operative state, the count value is simultaneously received by said random number generating circuit as the initial value.

Claim 51 (Currently Amended): An SD memory card system comprising:

a driver comprising a random number's seed generating circuit having an oscillator which generates a clock and a counter which operates in synchronism with the clock; and a

random number generating circuit which generates a random number using an initial value generated by said random number's seed generating circuit; and

an SD memory card driven by said driver and having a data protecting function,

wherein a count value of said counter is output in response to a signal asynchronous with the clock, the [output] count value is used as the initial value, and transfer data is kept secret using the random number, and

wherein said oscillator comprises a voltage-controlled oscillator having an external terminal, said oscillator and said external terminal are electrically disconnected before the count value is output, and said oscillator and said external terminal are electrically connected after the count value is output.

Claim 52 (Original): A system according to claim 51, wherein the random number is generated every time a power supply is turned on, every time the data is written or read, or every time a predetermined operation is performed by a user.

Claim 53 (Original): A system according to claim 51, wherein the signal is a signal output from a power-on reset circuit upon detecting that a power supply is turned on, and a power supply potential is stabilized.

Claim 54 (Original): A system according to claim 51, wherein the signal is an operation start signal output from a controller.

Claim 55 (Original): A system according to claim 54, wherein the operation start signal is output when the controller recognizes that a power supply is turned on.

Claim 56 (Original): A system according to claim 54, wherein the operation start signal is output when the controller recognizes that a predetermined operation is performed by a user.

Claim 57 (Original): A system according to claim 51, wherein said oscillator is set in an inoperative state or lowers a frequency of the clock after the count value is output in response to the signal.

Claim 58 (Canceled):

Claim 59 (Original): A system according to claim 58, wherein a switch circuit controlled by the signal is connected between said oscillator and the external terminal.

Claim 60 (Original): A system according to claim 58, wherein after the count value is output, the clock is used as a system clock.

Claim 61 (Original): A system according to claim 51, wherein a timing at which the count value is output changes within a range of time longer than a period of the clock every time the count value is output.

Claim 62 (Original): A system according to claim 51, further comprising a latch circuit which latches the count value on the basis of the signal,

wherein the count value latched by said latch circuit is used as the initial value.

Claim 63 (Original): A system according to claim 51, wherein when said random number generating circuit to which the signal is input is set in an operative state, the count value is simultaneously received by said random number generating circuit as the initial value.

Claim 64 (Currently Amended): An SD memory card system comprising:

a driver comprising a random number's seed generating circuit having an oscillator which generates a clock and a counter which operates in synchronism with the clock, and a random number generating circuit which generates a random number using an initial value generated by said random number's seed generating circuit;

and an SD memory card driven by said driver and having a data protecting function, wherein a timing at which a count value of said counter is output changes at random within a predetermined range in response to a signal, the [output] count value is used as the initial value, and transfer data is kept secret using the random number, and

wherein said oscillator comprises a voltage-controlled oscillator having an external terminal, said oscillator and said external terminal are electrically disconnected before the count value is output, and said oscillator and said external terminal are electrically connected after the count value is output.

Claim 65 (Original): A system according to claim 64, wherein the random number is generated every time a power supply is turned on, every time the data is written or read, or every time a predetermined operation is performed by a user.

Claim 66 (Original): A system according to claim 64, wherein the signal is a signal output from a power-on reset circuit upon detecting that a power supply is turned on, and a power supply potential is stabilized.

Claim 67 (Original): A system according to claim 64, wherein the signal is an operation start signal output from a controller.

Claim 68 (Original): A system according to claim 67, wherein the operation start signal is output when the controller recognizes that a power supply is turned on.

Claim 69 (Original): A system according to claim 67, wherein the operation start signal is output when the controller recognizes that a predetermined operation is performed by a user.

Claim 70 (Original): A system according to claim 64, wherein said oscillator is set in an inoperative state or lowers a frequency of the clock after the count value is output in response to the signal.

Claim 71 (Canceled).

Claim 72 (Original): A system according to claim 71, wherein a switch circuit controlled by the signal is connected between said oscillator and the external terminal.

Claim 73 (Original): A system according to claim 71, wherein after the count value is output, the clock is used as a system clock.

Claim 74 (Original): A system according to claim 64, wherein
a timing at which the count value is output changes within a range of time longer than a period of the clock every time the count value is output.

Claim 75 (Original): A system according to claim 64, further comprising a latch circuit which latches the count value on the basis of the signal
wherein the count value latched by said latch circuit is used as the initial value.

Claim 76 (Original): A system according to claim 64, wherein when said random number generating circuit to which the signal is input is set in an operative state, the count

value is simultaneously received by said random number generating circuit as the initial value.